

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application Of ) PATENT APPLICATION  
Inventors: Peijun Ding ) Docket No. AM-1776  
Tony Chiang )  
Barry L. Chin )  
Serial No.: Not Yet Assigned )  
Filed: Herewith )  
Title: A TAILORED BARRIER LAYER WHICH )  
PROVIDES IMPROVED COPPER )  
INTERCONNECT ELECTROMIGRATION )  
RESISTANCE )

CERTIFICATE OF MAILING BY "EXPRESS MAIL"  
UNDER 37 C.F.R. § 1.10

"EXPRESS MAIL" MAILING LABEL NUMBER: EI215419063US  
DATE OF DEPOSIT: December 19, 1997

I hereby certify that this correspondence is being deposited with  
the United States Postal Service, "Express Mail Post Office to  
Addressee" service under 37 CFR 1.10 with MAILING LABEL NUMBER  
filled in above, addressed to **The Assistant Commissioner for  
Patents, Box Patent Application, Washington, D.C. 20231**  
on the DATE OF DEPOSIT filled in above.

Kathi Rafayko (Signature)  
Kathi Rafayko, Reg. No. 36,544  
(Type Name)

Signature Date: December 19, 1997

**APPLICATION TRANSMITTAL LETTER**

Assistant Commissioner for Patents  
Washington, D.C. 20231  
**Attn: BOX PATENT APPLICATION**

Sir:

Transmitted herewith for filing is the patent application identified as follows:

Inventor(s): Peijun Ding  
Tony Chiang  
Barry L. Chin

Title: A TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED  
COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE

No. of pages of Specification: 16; No. of pages of Claims: 6; No. of pages of Abstract: 1

No. of Sheets of Drawings: 2; Formal:   , Informal: X.

Also enclosed are:

X A Declaration and Power of Attorney.

X An Assignment. Recording of the Assignment is hereby requested.

   A Power of Attorney.

   An Information Disclosure Statement under 37 C.F.R. §1.56.

### FEES DUE

The fees due for filing the specification pursuant to 37 C.F.R. §1.16 and for recording of the Assignment, if any, are determined as follows:

C L A I M S					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					\$ 790.00
Total Claims	31	MINUS 20=	11	x \$22 =	242.00
Independent Claims	5	MINUS 3 =	2	x \$82 =	164.00
If multiple dependent claims are presented, add \$270.00					270.00
Add Assignment Recording Fee of \$40.00 if Assignment document is enclosed					40.00
<b>TOTAL APPLICATION FEE DUE</b>					<b>1,506.00</b>

### PAYMENT OF FEES

- The full fee due in connection with this communication is \$1,506.00, and is provided as follows:
  - [x] Check No. 448 in the amount of \$1,506.00 is enclosed.
  - [x] The Commissioner is hereby authorized to charge any additional fees which may be due under 37 C.F.R. § 1.16(a), § 1.16(b), §1.16(c) or §.21(h) or to credit any overpayment to Deposit Account No. 01-1651 of Applied Materials, Inc. of Santa Clara, California. A duplicate copy of this authorization is enclosed.

456789 0123456789

Please direct all correspondence concerning the above-identified application to the following address:

Patent Counsel  
Applied Materials, Inc.  
P.O. Box 450-A  
Santa Clara, California 95052

Please direct telephone inquiries to:

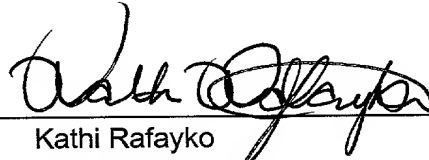
Shirley L. Church, Esq.  
(408) 745-1567

Respectfully submitted,

Date:

Dec 19, 1997

By:



Kathi Rafayko  
Agent for Applicants  
Reg. No. 36,644

265727-20756630

**United States Patent Application for:**

**A TAILORED BARRIER LAYER WHICH PROVIDES  
IMPROVED COPPER INTERCONNECT  
ELECTROMIGRATION RESISTANCE**

**Inventors: Peijun Ding**

**Tony Chiang**

**Barry L. Chin**

**Attorney Docket No. AM-1776**

---

**Certification Under 37 CFR 1.10**

I hereby certify that this New Patent Application and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date December 19, 1997 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EI215536970US addressed to the: Assistant Commissioner of Patents, Box Patent Application, Washington, D.C. 20231.

**Kathi Rafayko, Reg. No. 36,644**

**Person Mailing Paper**

  
Signature of Person Mailing Paper

A TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED  
COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE

**BACKGROUND OF THE INVENTION**

**1. Field of the Invention**

The present invention pertains to a particular TaN<sub>x</sub>/Ta barrier/wetting layer structure which increases the degree of {111} crystal orientation in an overlying copper layer, thereby providing improved electromigration resistance of the copper.

**2. Brief Description of the Background Art**

As microelectronics continue to miniaturize, interconnection performance, reliability, and power consumption has become increasingly important, and interest has grown in replacing aluminum alloys with lower-resistivity and higher-reliability metals. Copper offers a significant improvement over aluminum as a contact and interconnect material. For example, the resistivity of copper is about 1.67  $\mu\Omega\text{cm}$ , which is only about half of the resistivity of aluminum.

There are two principal competing technologies under evaluation by material and process developers working to enable the use of copper. The first technology is known as damascene technology. In this technology, a typical process for producing a multilevel structure having feature sizes (*i.e.*, width of the aperture) in the range of 0.5 micron ( $\mu\text{m}$ ) or less would include: blanket deposition of a dielectric material; patterning of the dielectric material to form openings; deposition of a diffusion barrier layer and, optionally, a wetting layer to line the openings; deposition of a copper layer onto the substrate in sufficient thickness to fill the openings; and removal of excessive conductive material from the substrate surface using chemical-mechanical polishing

1 (CMP) techniques. The damascene process is described in detail by C. Steinbruchel in  
2 "Patterning of copper for multilevel metallization: reactive ion etching and chemical-  
3 mechanical polishing", *Applied Surface Science* 91 (1995) 139 - 146.

4 The competing technology is one which involves the patterned etch of a copper  
5 layer. In this technology, a typical process would include deposition of a copper layer on  
6 a desired substrate (typically a dielectric material having a barrier layer on its surface);  
7 application of a patterned hard mask or photoresist over the copper layer; pattern etching  
8 of the copper layer using wet or dry etch techniques; and deposition of a dielectric  
9 material over the surface of the patterned copper layer, to provide isolation  
10 of conductive lines and contacts which comprise various integrated circuits.

11 Typically, the copper layer can be applied using sputtering techniques well  
12 known in the art. The sputtering of copper provides a much higher deposition rate than  
13 evaporation or CVD (chemical vapor deposition) and provides a purer copper film than  
14 CVD.

15 In integrated circuit interconnect structures where copper is the material used to  
16 form conductive lines and contacts, it is recognized that copper diffuses rapidly into  
17 adjacent layers of SiO<sub>2</sub> and silicon and needs to be encapsulated. Gang Bai et al. in  
18 "Copper Interconnection Deposition Techniques and Integration", 1996 Symposium on  
19 VLSI Technology, Digests of Technical Papers (0-7803-3342-X/96, IEEE), describe the  
20 effectiveness of Ta, TiN, W and Mo as barrier layers for use with copper. They  
21 concluded that Ta annealed in UHV (ultra high vacuum) after copper deposition  
22 provided the best barrier layer. Sputtered copper appeared to be preferable over CVD  
23 copper and over electroplated copper, although all the data for electroplated copper was  
24 not available at the time of presentation of the paper.

1 U.S. Patent No. 4,319,264 of Gangulee et al., issued March 9, 1982 and titled  
2 "Nickel-gold-nickel Conductors For Solid State Devices" discusses the problem of  
3 electromigration in solid state devices. In particular, the patent discusses the application  
4 of direct current over particular current density ranges which induces motion of the  
5 atoms comprising the thin film conductor, the effect known as electromigration.  
6 Electromigration is said to induce crack or void formation in the conductor which, over a  
7 period of time, can result in conductor failure. The rate of electromigration is said to be  
8 dependent on the current density imposed on the conductor, the conductor temperature,  
9 and the properties of the conductor material. In high current density applications,  
10 potential conductor failure due to electromigration is said to severely limit the reliability  
11 of the circuit. In discussing the various factors affecting performance of the conductive  
12 materials, grain structure is mentioned as being important. (In order to obtain adequate  
13 lithographic line width resolution, it is recommended that the film be small grained, with  
14 a grain size not exceeding about one-third of the required line width.) Uniformity of  
15 grain size and preferred crystallographic orientation of the grains are also said to be  
16 factors which promote longer (electromigration limited) conductor lifetimes. Fine  
17 grained films are also described as being smoother, which is a desirable quality in  
18 semiconductor applications, to lessen difficulties associated with covering the conductor  
19 with an overlayer.

20 U.S. Patent No. 5,571,752 to Chen et al., issued November 5, 1996, discloses a  
21 method for patterning a submicron semiconductor layer of an integrated circuit. In one  
22 embodiment describing an aluminum contact, titanium or titanium nitride having a  
23 thickness of between approximately 300 and 2,000 Å is formed by sputter deposition to  
24 reach the bottom of a contact opening. Finally, a second conductive layer, typically  
25 aluminum, is applied over the surface of the conformal conductive layer. The aluminum

1 is sputtered on, preferably at a temperature ranging between approximately 100°C and  
2 400°C. This method is said to make possible the filling of contact openings having  
3 smaller device geometry design requirements by avoiding the formation of fairly large  
4 grain sizes in the aluminum film.

5 As described in U.S. Patent Application Serial No. 08/824,911, of Ngan et al.,  
6 filed March 27, 1997 and commonly assigned with the present invention, efforts have  
7 been made to increase the {111} crystallographic content of aluminum as a means of  
8 improving electromigration of aluminum. In particular, the {111} content of an  
9 aluminum layer was controlled by controlling the thickness of various barrier layers  
10 underlying the aluminum layer. The underlying barrier layer structure was Ti/TiN/TiN<sub>x</sub>,  
11 which enabled aluminum filling of high aspect vias while providing an aluminum fill  
12 exhibiting the high degree of aluminum {111} crystal orientation. The Ti/TiN/TiN<sub>x</sub>  
13 barrier layer was deposited using IMP (ion metal plasma) techniques, and the barrier  
14 layer thicknesses were as follows. The thickness of the first layer of Ti ranges from  
15 greater than about 100 Å to about 500 Å (the feature geometry controls the upper  
16 thickness limit). The thickness of the TiN second layer ranges from greater than about  
17 100 Å to less than about 800 Å (preferably, less than about 600 Å). And, the TiN<sub>x</sub> third  
18 layer (having a Ti content ranging from about 50 atomic percent titanium to about 100  
19 atomic percent titanium) ranges from about 15 Å to about 500 Å. A Ti/TiN/TiN<sub>x</sub> barrier  
20 layer having this structure, used to line a contact via, is described as enabling complete  
21 filling of via with sputtered warm aluminum, where the feature size of the via or aperture  
22 is about 0.25 micron or less and the aspect ratio ranges from about 5 : 1 to as high as  
23 about 6 : 1.

24 Subsequently, in U.S. Patent Application Serial No. 08/924,487, of Ngan et al.,  
25 filed August 23, 1997 (Docket No. 1987), the inventors disclose that to maintain a



1 consistently high aluminum {111} crystal orientation content of an interconnect during  
2 the processing of a series of semiconductor substrates in a given process chamber, it is  
3 necessary to form the first deposited layer of the barrier layer to a minimal thickness of at  
4 least about 150 Å, to compensate for irregularities in the crystal orientation which may  
5 be present during the initial deposition of this layer when the process chamber is initially  
6 started up (and continuing for the first 7 - 8 wafers processed). Ngan et al. teach that in  
7 the case of a copper conductive layer, it may also be necessary that the first layer of a  
8 barrier layer structure underlying the copper layer have a minimal thickness of at least  
9 about 150 Å, to enable a consistent crystal orientation within the copper layer during the  
10 processing of a series of wafers in a semiconductor chamber.

#### 11 SUMMARY OF THE INVENTION

12 We have discovered that tantalum nitride ( $\text{TaN}_x$ ) is a better barrier layer for  
13 copper than tantalum (Ta). However, copper deposited directly over  $\text{TaN}_x$  does not  
14 exhibit a sufficiently high degree of {111} crystal orientation to provide the desired  
15 copper electromigration characteristics. We have developed a barrier layer structure  
16 comprising a layer of Ta overlying a layer of  $\text{TaN}_x$  which provides both a barrier to the  
17 diffusion of a copper layer deposited thereover, and enables the formation of a copper  
18 layer having a high {111} crystallographic content, so that copper electromigration  
19 resistance is increased.

20 The  $\text{TaN}_x$  layer, where x ranges from about 0.1 to about 1.5, is sufficiently  
21 amorphous to prevent the diffusion of copper into underlying silicon or silicon oxide  
22 surfaces. The desired thickness for the  $\text{TaN}_x$  layer is dependent on the device structure.  
23 For a typical interconnect, the  $\text{TaN}_x$  layer thickness ranges from about 50 Å to about  
24 1,000 Å. For a contact, the  $\text{TaN}_x$  layer, the thickness on the wall of a contact via ranges

1 from about 10 Å to about 300 Å, depending on the feature size. The TaN<sub>x</sub> layer is  
2 preferably deposited using standard reactive ion sputtering techniques at a substrate  
3 temperature ranging from about 20°C to about 500°C. However, ion deposition  
4 sputtering techniques may be used to deposit this layer.

5 The Ta layer deposited over the TaN<sub>x</sub> layer has a desired thickness ranging from  
6 about 5 Å to about 500Å, wherein the thickness is preferably greater than about 20 Å,  
7 depending on the feature size. The Ta layer is preferably deposited using standard ion  
8 sputtering techniques at a substrate temperature ranging from about 20°C to about  
9 500°C. However, ion deposition sputtering techniques may be used to deposit this layer.

10 The copper layer is deposited at the thickness desired to suit the needs of the  
11 device. The copper layer may be deposited using any of the preferred techniques known  
12 in the art. Preferably, the entire copper layer or at least a "seed" layer of copper is  
13 deposited using physical vapor deposition techniques such as sputtering or evaporation,  
14 as opposed to CVD. Since the crystal orientation of the copper is sensitive to deposition  
15 temperature, it is important that the maximum temperature of the copper either during  
16 deposition or during subsequent annealing processes not be higher than about 500°C.  
17 Preferably, the maximum temperature is about 300°C.

#### 18 BRIEF DESCRIPTION OF THE DRAWINGS

19 Figure 1 shows a schematic of a cross sectional view of a sputtering chamber of  
20 the kind which can be used to deposit the barrier layer of the present invention.

21 Figure 2 shows a graph representative of the copper {111} crystal orientation on  
22 a TaN<sub>x</sub>/Ta barrier layer as a function of the thickness of the Ta layer, with the TaN<sub>x</sub> layer  
23 held constant at about 500 Å.

2        The present disclosure pertains to a TaN<sub>x</sub>/Ta/Cu structure and a method of  
3        creating that structure. The TaN<sub>x</sub>/Ta barrier layer structure enables the deposition of an  
4        overlying copper layer having a high {111} crystallographic content, so that  
5        electromigration resistance of the copper is increased.

As a preface to the detailed description, it should be noted that, as used in this specification and the appended claims, the singular forms "a", "an", and "the" include plural referents, unless the context clearly dictates otherwise. Thus, for example, the term "a semiconductor" includes a variety of different materials which are known to have the behavioral characteristics of a semiconductor, reference to a "plasma" includes a gas or gas reactants activated by an RF glow discharge, reference to "the contact material" or "interconnect material" includes copper and copper alloys, and other conductive materials which have a melting point enabling them to be sputtered over the temperature range described herein.

The term "aspect ratio" refers to the ratio of the height dimension to the width dimension of particular openings into which an electrical contact is to be placed. For example, a via opening which typically extends in a tubular form through multiple layers has a height and a diameter, and the aspect ratio would be the height of the tubular divided by the diameter. The aspect ratio of a trench would be the height of the trench divided by the minimal travel width of the trench at its base.

1 The term "contact via" or "via" refers to an electrical contact having an aspect  
2 ratio which is typically greater than 1:1. A contact via most frequently extends through  
3 multiple layers of material to connect one electrically conductive element with another.

4 The term "copper" includes alloys of copper of the kind typically used in the  
5 semiconductor industry. The preferred embodiments described herein were for a copper  
6 alloy comprising about 98% by weight copper.

7 The term "feature" refers to contacts, vias, trenches, and other structures which  
8 make up the topography of the substrate surface.

9 The term "interconnect" generally refers to conductive structures within a  
10 semiconductive device. For purposes of this patent application, electrical contacts in the  
11 form of a "contact via" or "via" (which has a higher aspect ratio than conductive lines in  
12 trenches, for example) is distinguished from other conductive structures which form  
13 interconnects.

14 The term "ion-deposition sputtered" and the term "reactive ion metal plasma  
15 (IMP)" refer to sputter deposition using a particular technique, wherein a high density,  
16 inductively coupled RF plasma is positioned between the sputtering cathode and the  
17 substrate support electrode, whereby at least a portion of the sputtered emission is in the  
18 form of ions at the time it reaches the substrate surface. Typically, 10% or more of the  
19 sputtered emission is in the form of ions at the time it reaches the substrate surface.

20 The term "traditional sputtering" refers to a method of forming a film layer on a  
21 substrate wherein a target is sputtered and the material sputtered from the target passes  
22 between the target and the substrate to form a film layer on the substrate, and no means is  
23 provided to ionize a substantial portion of the target material sputtered from the target  
24 before it reaches the substrate. One apparatus configured to provide traditional  
25 sputtering is disclosed in U.S. Patent No. 5,320,728, the disclosure of which is

1 incorporated herein by reference. In such a traditional sputtering configuration, the  
2 percentage of target material which is ionized is less than 10%, more typically less than  
3 1%, of that sputtered from the target.

4 The term "XRD" (X-ray Diffraction) refers to a technique commonly used to  
5 measure crystalline orientation, wherein radiation over particular wavelengths is passed  
6 through the material to be characterized, and the diffraction of the radiation, caused by  
7 the material through which it passes, is measured. A map is created which shows the  
8 diffraction pattern, and the crystal orientation is calculated based on this map.

9 A "traditionally sputtered" tantalum nitride-comprising film or layer is deposited  
10 on a substrate by contacting a tantalum target with a plasma created from an inert gas  
11 such as argon in combination with nitrogen gas. A portion of the tantalum sputtered  
12 from the target reacts with nitrogen gas which has been activated by the plasma to  
13 produce tantalum nitride, and the gas phase mixture contacts the substrate to form a layer  
14 on the substrate.

15

## 16 II. AN APPARATUS FOR PRACTICING THE INVENTION

17 A process system in which the method of the present invention may be carried  
18 out is the Applied Materials, Inc. (Santa Clara, California) Endura® Integrated  
19 Processing System. This process system is not specifically shown in the Figures.  
20 However, the system is generally known in the semiconductor processing industry and is  
21 shown and described in United States Patents Nos. 5,186,718 and 5,236,868, the  
22 disclosures of which are incorporated by reference. A schematic of a typical sputtering  
23 apparatus useful in forming the smooth-surfaced  $\text{TaN}_x/\text{Ta}$  barrier layer of the present  
24 invention is shown in Figure 1. Sputtering apparatus 100 includes a sputtering target 110  
25 which has two major surfaces, a back surface 112 from which heat is removed, and a

1 front surface 114 which is the sputtering surface. The sputtered material is deposited on  
2 the surface of semiconductor workpiece 116 which is supported on platen 118. The  
3 spacing between the workpiece 116 and the target 110 may be adjusted by moving the  
4 platen 118. The sputtering target (cathode) 110 operates at power levels up to about 24  
5 kW. An ionized gas, typically generated from an inert gas such as argon is used to  
6 impact sputtering target 110, to produce sputtered metal atoms which are deposited on  
7 workpiece 116. The inert gas enters vacuum chamber 117 in the vicinity to target 112  
8 through openings which are not shown on Figure 1. Additional gas may enter vacuum  
9 chamber 117 from the surface of workpiece support platen 118, which includes openings  
10 (not shown) in its surface to permit the flow of heat transfer gas between workpiece 116  
11 and support platen 118. Such gases are evacuated through an opening (not shown) in  
12 vacuum chamber 117, which opening is connected to a conduit (not shown) leading to a  
13 vacuum pump (not shown). Vacuum chamber 117 can be operated at pressures ranging  
14 from about 0.1 mT to about 60 mT, depending on the particular process involved.

### 15 III. A METHOD FOR PRACTICING THE INVENTION

#### 16 EXAMPLE ONE: FORMATION OF A $\text{TaN}_x$ /Ta BARRIER LAYER

17 To form the  $\text{TaN}_x$ /Ta barrier layer structure, a tantalum target cathode 110 was  
18 used, and a DC power was applied to this cathode over a range from about 0.5 kW to  
19 about 8 kW. The spacing between target cathode 110 and workpiece 116 was  
20 approximately 200 - 300 mm. During the formation of the  $\text{TaN}_x$  first layer, argon gas  
21 feed to vacuum chamber 117 was about 15 sccm to the substrate support platen 118 and  
22 about 7 sccm to the openings in the vicinity of target cathode 110. Nitrogen gas was also  
23 fed into vacuum chamber 117 in the vicinity of target cathode 110. The nitrogen gas  
24 feed rate ranged from about 2 to about 20 sccm, depending on the DC power applied,

1 with the nitrogen feed rate being increased as the DC power was increased. With the DC  
2 power set at 4 kW and a nitrogen feed rate of about 14 sccm, the TaN<sub>x</sub> layer produced  
3 was TaN<sub>0.7</sub>, containing about 40 atomic percent nitrogen.

4 The substrate 116 was a 200 mm diameter silicon wafer having a silicon dioxide  
5 dielectric layer on its surface. The substrate was placed a distance of about 10 inches  
6 (25 cm) from target cathode 110. The operational pressure in vacuum chamber 117 was  
7 about 1.7 mT, and the substrate temperature of the silicon wafer was about 25°C. Under  
8 these conditions, a 500 Å thick layer of TaN was applied in approximately one minute.

9 Subsequent to application of the TaN layer, the nitrogen gas was shut off, the  
10 power to tantalum target cathode 110 was reduced from about 4 kW to about 1 kW, and  
11 the argon gas feed was maintained. The pressure in the vacuum chamber remained at  
12 about 1.7 mT, and the substrate temperature remained at about 25°C. Under these  
13 conditions, a 60 Å thick layer of tantalum was formed over the TaN layer in about  
14 10 seconds.

15 The data generated in Figure 2 was for TaN/Ta barrier layers produced in the  
16 manner described above, where the length of time for tantalum deposition was increased  
17 to produce a thicker tantalum layer, as appropriate.

## 18 EXAMPLE TWO: FORMATION OF THE COPPER CONDUCTIVE LAYER

19 The copper layer overlying the TaN barrier layer was applied using the same  
20 apparatus described with regard to application of the TaN barrier layer. The target  
21 cathode 110 was copper. During the formation of the overlying Cu layer, argon gas feed  
22 to vacuum chamber 117 was about 15 sccm to the substrate support platen 118 and about  
23 90 sccm to the openings in the vicinity of target cathode 110. The substrate, having a  
24 tantalum layer as its upper surface, was placed a distance of about 10 inches (25 cm)

1 from target cathode 110. The operational pressure in vacuum chamber 117 was about  
2 1.0 mT, and the substrate temperature was about 150°C. Under these conditions, a  
3 1,000 Å thick layer of copper was applied in about one minute.

4 With reference to the formation of the  $\text{TaN}_x/\text{Ta}/\text{Cu}$  structure in general, it is  
5 advisable to use the minimal thickness possible for the tantalum layer, as a flatter  
6 structure is preferred for planarization and imaging purposes, and it is difficult to remove  
7 excess tantalum from the surface of the workpiece. When chemical mechanical  
8 polishing is used to remove material on the surface of the workpiece between features  
9 (known as the "field"), the removal rate for tantalum is much slower than the copper  
10 removal rate. As a result, in order to ensure complete removal of copper and  $\text{Ta}/\text{TaN}_x$   
11 from the field, the copper may be over polished, creating a "dishing effect" in the area of  
12 a contact, where the copper is removed from the contact to a level below the surface of  
13 the substrate/workpiece. In addition, there is a cost in substrate processing time.

14 The minimal thickness for the tantalum layer is determined by the desired  
15 performance features for the layer. The layer must be sufficiently thick to provide a  
16 tantalum {002} crystalline orientation which enables easy wetting of the tantalum  
17 surface by the copper and depositing of a copper layer having a high {111} crystal  
18 orientation. Although a higher temperature is required to dewet/delaminate a depositing  
19 copper layer from a Ta surface than from a  $\text{TaN}_x$  surface, copper delamination is a  
20 problem in some instances. Typically, the copper layer is deposited at temperatures in  
21 the range of about 300°C to about 500°C (or a copper seed layer is deposited at lower  
22 temperatures, but additional copper is deposited and the combination is annealed at  
23 temperatures in this range), where delamination of the copper layer is a real possibility.  
24 When the copper is deposited for flat interconnect lines, the wetting criteria is not as  
25 important as it is when the copper is deposited to fill a contact via having a high aspect



1 ratio (*i.e.*, depth greater than width).

2 As the thickness of the tantalum layer increases, the wetting of the tantalum by a  
3 layer of copper applied thereover generally improves. As the thickness of the tantalum  
4 layer increases, the copper {111} crystallographic content generally increases as well.

5 The limitation on tantalum layer thickness is defined by the device feature size, in  
6 particular. If the  $TaN_x$  or the Ta layer is too thick, the overall resistance of the  
7 conductive feature increases. If these layers are too thin, the barrier may not be adequate  
8 to prevent diffusion; further, if the Ta layer is too thin, the copper {111} crystallographic  
9 content may be inadequate to provide the desired electromigration resistance.

10 In general, the copper {111} crystallographic content is poorer when copper is  
11 applied directly over a  $TaN_x$  layer due to the amorphous structural content of the  $TaN_x$   
12 layer. Further, copper applied by means other than sputtering, where the copper layer  
13 itself has a higher impurity level (such as copper applied by CVD), may result in an  
14 unacceptably low copper {111} crystallographic content. The use of a Ta layer over the  
15  $TaN_x$  layer can produce an acceptable surface for growth of a high copper {111}  
16 crystallographic content. Deposition of a seed layer of copper over the Ta surface prior  
17 to application of the entire copper contact by other means, such as CVD, provides a  
18 starting matrix for copper growth, since some CVD precursors and electroplating require  
19 a conductive substrate for the copper deposition process to take place. Further, the  
20 copper seed layer promotes an increase in the copper {111} crystallographic content.

21 IV. THE STRUCTURE OF THE  $TaN_x$ /Ta BARRIER LAYER AND ITS  
22 EFFECT ON THE COPPER {111} CRYSTALLOGRAPHIC CONTENT

23 Figure 2 shows a graph 200 of the {111} crystallographic content (measured by  
24 XRD) of a copper layer as a function of the thickness of the Ta layer of a  $TaN_x$ /Ta barrier  
25 layer.

1 In particular, the various specimens examined (prepared using the method  
2 described above) are represented on the scale labeled 207. The layers of material were  
3 deposited using standard, traditional sputtering techniques. In all instances, the copper  
4 layer was 1,000 Å thick. In all instances, except the data point labeled 206, the  
5 underlying layer of  $\text{TaN}_x$  was 500 Å thick. The data point labeled 206 represents a 500 Å  
6 thick Ta (only) barrier layer. The data point labeled 208 represents a 500 Å thick  $\text{TaN}_x$   
7 (only) barrier layer. The data point labeled 210 represents the  $\text{TaN}_x/\text{Ta}$  structure where  
8 the overlying Ta layer was 57 Å thick. The data point labeled 212 represents the  
9  $\text{TaN}_x/\text{Ta}$  structure where the overlying Ta layer was 114 Å thick. The data point labeled  
10 214 represents the  $\text{TaN}_x/\text{Ta}$  structure where the overlying Ta layer was 170 Å thick. The  
11 data point labeled 216 represents the  $\text{TaN}_x/\text{Ta}$  structure where the overlying Ta layer was  
12 227 Å thick. And, the data point labeled 218 represents the  $\text{TaN}_x/\text{Ta}$  structure where the  
13 overlying Ta layer was 456 Å thick.

14 The XRD scanning of these specimens was done using the standard  $\theta - 2\theta$   
15 technique, with the relative normalized area under the Cu {111} intensity peak shown on  
16 the scale labeled 203. Curve 202 illustrates the normalized area under the Cu {111} CPS  
17 (counts per second) intensity peak for the specimens previously described, with the Ta  
18 layer thickness increasing from left to right on the curve beginning with data point 210.  
19 A second measurement indicating the amount of the Cu {111} orientation present is  
20 provided in the rocking curve data shown on the scale labeled 205. The data represents  
21 the Cu {111} FWHM measured in degrees  $\theta$ .

22 In the rocking curve measurement technique, the sample is rotating and the  
23 detector is rotating. The CPS measurement is made at a set angle and then the detector is  
24 slightly rotated and a new CPS is measured. A plot of the CPS at increasing angle of  
25 measurement is made, generating a distribution curve of the quantity of the specific

1 crystal orientation measured at increasing angles.

2 FWHM = full width half max. FWHM is calculated by measuring the width of  
3 the curve at a position on the curve which represents one half of the maximum height of  
4 the curve. The FWHM is expressed in degrees and represents the number of degrees  
5 spanned by the width of the curve at half of its maximum height. A wider curve (a  
6 higher number on the scale), spanning a larger number of degrees, indicates that the  
7 signal for the crystallographic orientation of interest is not a strong signal and less copper  
8 {111} crystallographic orientation is present. A narrow curve (a lower number on the  
9 scale), spanning a limited number of degrees, is a strong signal, indicating a larger  
10 quantity of the crystallographic orientation is present. Curve 204 illustrates the FWHM  
11 for the specimens previously described, with the Ta layer thickness increasing from left  
12 to right on the curve beginning with data point 210.

13 Data point 206 on curve 202 shows the normalized area under the Cu {111}  
14 intensity peak for the specimen having a 500 Å thick Ta layer underlying the 1,000 Å  
15 thick sputtered copper layer. As is evident from the curve 202, the quantity of Cu {111}  
16 crystal orientation is relatively high. However, as previously mentioned, a layer of pure  
17 Ta does not provide a diffusion barrier which performs as well as the TaN<sub>x</sub>/Ta barrier  
18 layer structure in preventing copper diffusion into the underlying silicon dioxide  
19 dielectric layer.

20 Data point 208 on curve 202 shows the normalized area under the Cu {111}  
21 intensity peak for the specimen having a 500 Å thick TaN layer underlying the 1,000 Å  
22 thick sputtered copper layer. Although the TaN layer provides a good diffusion barrier,  
23 the quantity of Cu {111} is minimal. Data points 210 through 216 on curve 202 show  
24 the normalized area under the Cu {111} intensity peak for specimens having a 500 Å  
25 thick TaN layer, with increasing thicknesses of an overlying Ta layer (as the data point

1 number increases), all with a 1,000 Å layer of copper applied over the TaN/Ta barrier  
2 layer. The 500 Å TaN/57 Å Ta barrier layer of data point 210 provides about 10% less  
3 area under the Cu {111} peak than the 500 Å layer of Ta provided. The exact  
4 significance of this decrease in electromigration performance has not yet been  
5 determined; however, the difference is not expected to have a significant influence on  
6 device performance.

7 At data point 214 on curve 202, which represents the 500 Å TaN/170 Å Ta barrier  
8 layer, the area under the Cu {111} peak is equivalent to the pure layer of Ta.  
9 Surprisingly, at some point between the 500 Å TaN/227 Å Ta barrier layer represented  
10 by data point 216 and the 500 Å TaN/456 Å Ta barrier layer represented by data point  
11 218, the Cu {111} crystal content increases drastically, rising to a value about 20%  
12 greater than that for the pure layer of Ta. The FWHM data shown on curve 204 for the  
13 same specimens described above confirms the same trends illustrated by the normalized  
14 area under the Cu {111} intensity peak. See, for example, a lower FWHM after data  
15 point 216 on curve 204, indicating an increased amount of the copper {111}  
16 crystallographic orientation.

17 Based on this disclosure, one skilled in the art can provide a barrier layer which  
18 prevents the diffusion of a copper layer deposited thereover, and enable the formation of  
19 a copper layer having a high {111} crystallographic content.

20 The above described preferred embodiments are not intended to limit the scope  
21 of the present invention, as one skilled in the art can, in view of the present disclosure  
22 expand such embodiments to correspond with the subject matter of the invention claimed  
23 below.

## CLAIMS

We claim:

- 1 1. A barrier layer for use in combination with a conductive layer, said barrier layer  
2 having a particular structure comprising:
  - 3 a) a first layer of  $\text{TaN}_x$  having a thickness ranging from greater than about 10 Å  
4 to about 1,000 Å; and
  - 5 b) a second layer of Ta overlying said first layer and having a thickness ranging  
6 from about 5 Å to about 500 Å.
- 1 2. The barrier layer of Claim 1, wherein the conductive layer is copper.
- 1 3. The barrier layer of Claim 1, wherein said barrier layer is used in an interconnect  
2 structure, and wherein the thickness of said  $\text{TaN}_x$  layer ranges from about 50 Å to about  
3 1,000 Å and the thickness of said Ta layer ranges from about 20 Å to about 500 Å.
- 4 4. The barrier layer of Claim 1, wherein said barrier layer is used in a contact via  
5 structure, and wherein the thickness of said  $\text{TaN}_x$  layer ranges from about 10 Å to about  
6 300 Å and the thickness of said Ta layer ranges from about 5 Å to about 300 Å.
- 7 5. The barrier layer of Claim 2, or Claim 3, or Claim 4, wherein x ranges from about 0.1  
1 to about 1.5.  
2

1 6. A copper interconnect structure comprising the barrier layer of Claim 2 and an  
2 overlying copper layer, wherein the Cu {111} crystallographic content of said overlying  
3 copper layer is at least 70% of the Cu {111} crystallographic content which can be  
4 obtained using a pure Ta barrier layer which is about 500 Å thick.

1 7. A copper contact via-comprising structure including the barrier layer of Claim 2 and a  
2 copper fill, wherein the copper fill layer Cu {111} crystallographic content is at least  
3 70% of the Cu {111} crystallographic content which can be obtained using a pure Ta  
4 barrier layer which is about 250 Å thick.

1 8. A method of producing a barrier layer useful in combination with a conductive layer,  
2 said method comprising the steps of:

3 a) depositing a first layer of  $TaN_x$  having a thickness ranging from greater than  
4 about 10 Å to about 1,000 Å; and

5 b) depositing a second layer of Ta having a thickness ranging from about 5 Å to  
6 about 500 Å.

1 9. The method of Claim 8, wherein the conductive layer is copper.

1 10. The method of Claim 8, wherein said first layer of  $TaN_x$  is deposited upon a  
2 substrate having a substrate temperature ranging from about 25°C to about 500°C.

1 11. The method of Claim 8, wherein said second layer of Ta is deposited upon a  
2 substrate having a substrate temperature ranging from about 25°C to about 500°C.

1 12. The method of Claim 8, wherein said barrier layer is used in an interconnect  
2 structure, and wherein the thickness of said TaN<sub>x</sub> layer ranges from about 50 Å to about  
3 1,000 Å and the thickness of said Ta layer ranges from about 20 Å to about 500 Å.

1 13. The method of Claim 8, wherein said barrier layer is used in a contact via structure,  
2 and wherein the thickness of said TaN<sub>x</sub> layer ranges from about 10 Å to about 300 Å and  
3 the thickness of said Ta layer ranges from about 5 Å to about 300 Å.

1 14. The method of Claim 8, or Claim 12, or Claim 13, where x ranges from about 0.1 to  
2 about 1.5.

1 15. The method of Claim 8, wherein at least a portion of said Ta layer is deposited using  
2 a traditional, standard sputtering technique.

1 16. The method of Claim 12, wherein at least a portion of said Ta layer is deposited  
2 using a traditional, standard sputtering technique.

1 17. The method of Claim 8, wherein at least a portion of the TaN<sub>x</sub> layer is deposited  
2 using a traditional, standard sputtering technique.

1 18. The method of Claim 8, wherein at least a portion of said Ta layer is deposited using  
2 ion-deposition sputtering.

1 19. The method of Claim 13, wherein at least a portion of said Ta layer is deposited  
2 using ion-deposition sputtering.

1 20. The method of Claim 8, wherein at least a portion of the  $\text{TaN}_x$  layer is deposited  
2 using ion-deposition sputtering.

1 21. A method of producing a copper interconnect structure comprising the barrier layer  
2 of Claim 1 and an overlying copper layer, wherein the Cu {111} crystallographic content  
3 of said overlying copper layer is at least 70 % of the Cu {111} crystallographic content  
4 which can be obtained by depositing said copper layer using a pure Ta barrier layer  
5 which is about 500 Å thick, said method comprising the steps of:

6 a) depositing a first layer of  $\text{TaN}_x$  having a thickness ranging from greater than  
7 about 50 Å to about 1,000 Å;

8 b) depositing a second layer of Ta having a thickness ranging from about 5 Å to  
9 about 500 Å over the surface of said first layer of  $\text{TaN}_x$ ; and

10 c) depositing a third layer of copper over the surface of said second layer of Ta,  
11 wherein at least a portion of said third layer of copper is deposited using a physical vapor  
12 deposition technique, and wherein the substrate temperature at which said third layer of  
13 copper is deposited is less than about 500°C.

1 22. The method of Claim 21, wherein said copper interconnect structure is annealed at a  
2 temperature of less than about 500°C.



1 23. A method of producing a copper-comprising contact via structure comprising the  
2 barrier layer of Claim 1 and an overlying copper layer, wherein the Cu {111}  
3 crystallographic content of said overlying copper layer is at least 70% of the Cu {111}  
4 crystallographic content which can be obtained by depositing said copper layer using a  
5 pure Ta barrier layer which is about 300 Å thick, said method comprising the steps of:

6 a) depositing a first layer of TaN<sub>x</sub> having a thickness ranging from greater than  
7 about 10 Å to about 300 Å;

8 b) depositing a second layer of Ta having a thickness ranging from about 5 Å to  
9 about 300 Å over the surface of said first layer of TaN<sub>x</sub>; and

10 c) depositing a third layer of copper over the surface of said second layer of Ta,  
11 wherein at least a portion of said third layer of copper is deposited using a physical vapor  
12 deposition technique, and wherein the substrate temperature at which said third layer of  
13 copper is deposited is less than about 500°C.

1 24. The method of Claim 23, wherein said contact-comprising structure is annealed at a  
2 temperature of less than about 500°C.

1 25. The method of Claim 23, wherein said copper layer is deposited at a temperature of  
2 less than about 300°C.

1 26. The method of Claim 25, wherein said structure is annealed at a temperature of less  
2 than about 500°C.

1 27. A method of producing a copper-comprising contact structure including the barrier  
2 layer of Claim 1 and an overlying copper layer, wherein the Cu {111} crystallographic  
3 content of said overlying copper layer is at least 70% of the Cu {111} crystallographic  
4 content which can be obtained by depositing said copper layer using a pure Ta barrier  
5 layer which is about 300 Å thick, said method comprising the steps of:

6 a) depositing a first layer of TaN<sub>x</sub> having a thickness ranging from greater than  
7 about 10 Å to about 300 Å;

8 b) depositing a second layer of Ta having a thickness ranging from about 5 Å to  
9 about 300 Å over the surface of said first layer of TaN<sub>x</sub>; and

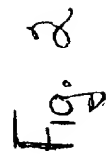
10 c) depositing a third layer of copper over the surface of said second layer of Ta,  
11 wherein at least a portion of said third layer of copper is deposited using a physical vapor  
12 deposition technique, and wherein the substrate temperature at which said third layer of  
13 copper is deposited is less than about 500°C,

14 wherein at least a portion of said first layer, or said second layer, or said third  
15 layer, or a combination thereof, is deposited using ion-deposition sputtering.

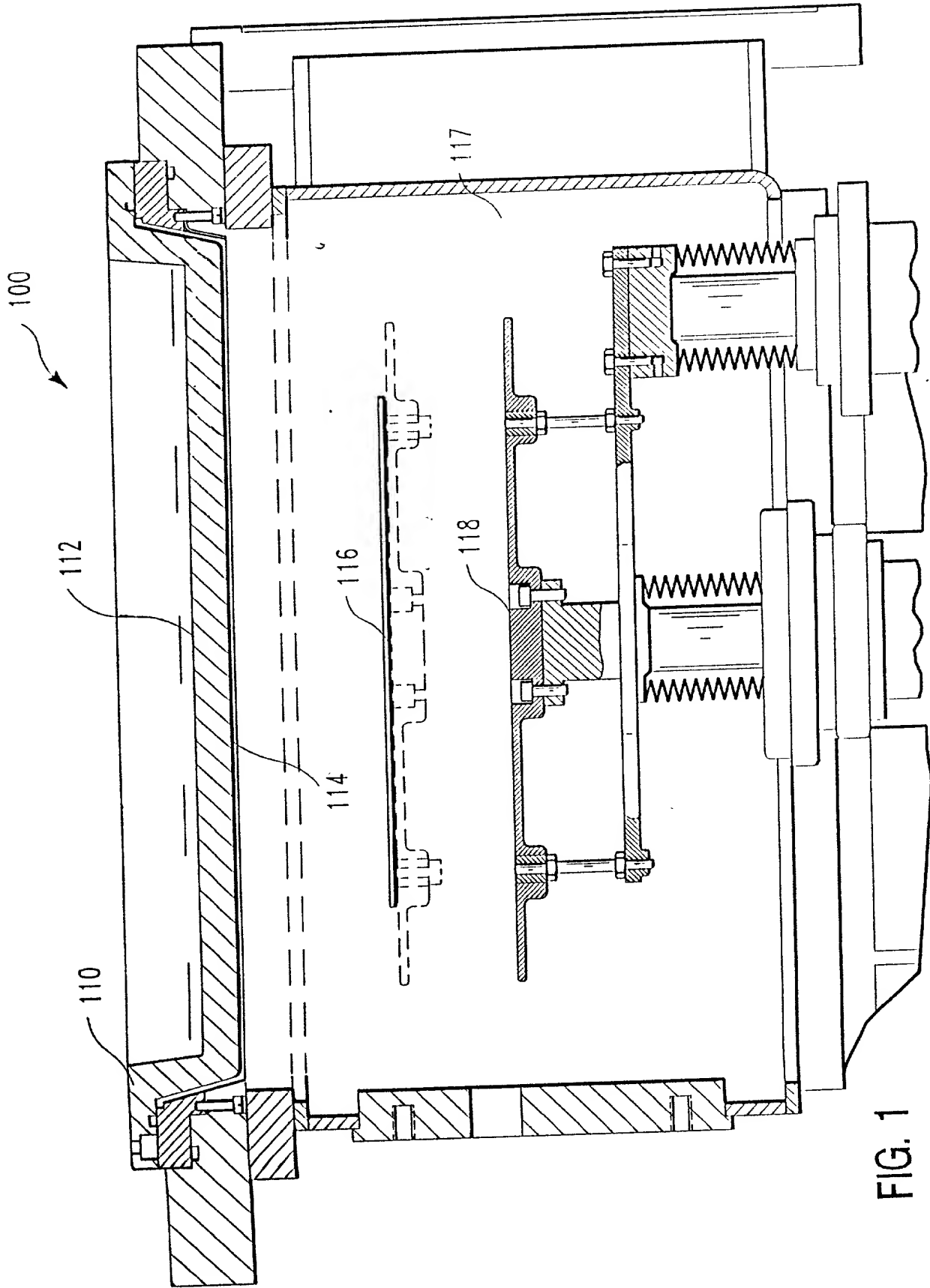
**ABSTRACT OF THE DISCLOSURE**

Disclosed herein is a barrier layer structure useful in forming copper interconnects and electrical contacts of semiconductor devices. The barrier layer structure comprises a first layer of  $\text{TaN}_x$  which is applied directly over the substrate, followed by a second layer of Ta. The  $\text{TaN}_x$ /Ta barrier layer structure provides both a barrier to the diffusion of a copper layer deposited thereover, and enables the formation of a copper layer having a high {111} crystallographic content so that the electromigration resistance of the copper is increased. The  $\text{TaN}_x$  layer, where x ranges from about 0.1 to about 1.5, is sufficiently amorphous to prevent the diffusion of copper into the underlying substrate, which is typically silicon or a dielectric such as silicon dioxide. The thickness of the  $\text{TaN}_x$  and Ta layers used for an interconnect depend on the feature size and aspect ratio; typically, the  $\text{TaN}_x$  layer thickness ranges from about 50 Å to about 1,000 Å, while the Ta layer thickness ranges from about 20 Å to about 500 Å. For a contact via, the permissible layer thickness on the via walls must be even more carefully controlled based on feature size and aspect ratio; typically, the  $\text{TaN}_x$  layer thickness ranges from about 10 Å to about 300 Å, while the Ta layer thickness ranges from about 5 Å to about 300 Å. The copper layer is deposited at the thickness desired to suit the needs of the device. The copper layer may be deposited using any of the preferred techniques known in the art. Preferably, the entire copper layer, or at least a "seed" layer of copper, is deposited using physical vapor deposition techniques such as sputtering or evaporation, as opposed to CVD or electroplating. Since the crystal orientation of the copper is sensitive to deposition temperature, and since the copper may tend to dewet/delaminate from the barrier layer if the temperature is too high, it is important that the copper be deposited and/or annealed at a temperature of less than about 500°C, and preferably at a temperature of less than about 300°C.

## XRD of Cu {111} on TaN<sub>x</sub>/Ta Substrate



266T2T" 80T5680



**PATENT APPLICATION****DECLARATION AND POWER OF ATTORNEY**  
**Original Application**

As below named inventor, I declare that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in this Declaration, that the information given herein is true, that I believe that I am the original, first and sole inventor of the invention entitled:

**A TAILORED BARRIER LAYER WHICH PROVIDES IMPROVED COPPER INTERCONNECT ELECTROMIGRATION RESISTANCE**

which is described and claimed in:

X the attached specification or

the specification in application Serial No. \_\_\_\_\_ filed \_\_\_\_\_ amended \_\_\_\_\_

that I acknowledge my duty to disclose information in accordance with 37 C.F.R. Section 1.56 and defined on the attached sheet, which is material to the examination of this application, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, or in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application and that as to applications for patent or inventor's certificate filed by me or my legal representatives or assigns in any country foreign to the United States of America, the earliest filed foreign applications(s) filed within twelve months prior to the filing date of this application and all foreign applications filed more than twelve months prior to the filing date of this application, if any, are identified below.

**CHECK APPROPRIATE BOX:**

X No earlier-filed foreign applications.

Required information as to foreign applications filed prior to filing date of this application is on page 5 attached hereto and made a part hereof.

# POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

NAME	REGISTRATION NO.
Michael L. Sherrard	<u>28,041</u>
Peter J. Sgarbossa	<u>25,610</u>
Donald J. Verplancken	<u>33,217</u>
Michael B. Einschlag	<u>29,301</u>
Lawrence Edelman	<u>25,225</u>

NAME	REGISTRATION NO.
Raymond Kam-On Kwong	<u>37,165</u>
Leslie Weise	<u>36,305</u>
James C. Wilson	<u>35,412</u>
Shirley L. Church	<u>31,858</u>
Kathi Rafayko	<u>36,644</u>

## SEND CORRESPONDENCE TO:


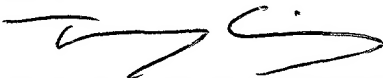
Patent Counsel  
Applied Materials, Inc.  
P.O. Box 450-A  
Santa Clara, California 95052

## DIRECT TELEPHONE CALLS TO:

Shirley L. Church, Esq.  
(408) 745-1567

(201) FULL NAME OF INVENTOR	LAST NAME Ding	FIRST NAME Peijun	MIDDLE NAME	
RESIDENCE & CITIZENSHIP	CITY San Jose	STATE OR FOREIGN COUNTRY California	COUNTRY OF CITIZENSHIP People's Republic of China	
POST OFFICE ADDRESS	POST OFFICE ADDRESS 1020 W. Riverside Way	CITY San Jose	STATE OR COUNTRY California	ZIP CODE 95129
(202) FULL NAME OF INVENTOR	LAST NAME Chiang	FIRST NAME Tony	MIDDLE NAME	
RESIDENCE & CITIZENSHIP	CITY Mountain View	STATE OR FOREIGN COUNTRY California	COUNTRY OF CITIZENSHIP U.S.A.	
POST OFFICE ADDRESS	POST OFFICE ADDRESS 100 N. Whisman Road, #17	CITY Mountain View	STATE OR COUNTRY California	ZIP CODE 94043
(203) FULL NAME OF INVENTOR	LAST NAME Chin	FIRST NAME Barry	MIDDLE NAME L	
RESIDENCE & CITIZENSHIP	CITY Saratoga	STATE OR FOREIGN COUNTRY California	COUNTRY OF CITIZENSHIP U.S.A.	
POST OFFICE ADDRESS	POST OFFICE ADDRESS 13174 Cumberland Drive	CITY Saratoga	STATE OR COUNTRY California	ZIP CODE 95070
(204) FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME	
RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP	
POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Name (201) NAME: Peijun Ding	Signature 	Date 12/18/97
Name (202) NAME: Tony Chiang	Signature 	Date 12/18/97
Name (203) NAME: Barry L. Chin	Signature Barry L. Chin	Date 12/19/97
Name (204) NAME:	Signature	Date

#### Section 1.56 Duty to Disclose Information Material to Patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by Sections 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applications to carefully examine:

- (1) prior art cited in search reports of a foreign patent office in a counterpart application, and
- (2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and



(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the application takes in:

- (i) opposing an argument of unpatentability relied on by the Office, or
- (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any considerations given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

- (1) Each inventor named in the application;
- (2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent or inventor.

266727-8075680